Claims

What is claimed is:

1. A chip rate base band processor which receives digital information containing symbol information and provides a symbol output, comprising:

an input memory which stores the digital information;

a data PN code buffer;

a pilot PN code buffer;

a pilot multiplier having a first input coupled to the pilot PN code buffer, a second input coupled to the input memory, and an output;

a data multiplier having a first input coupled to the data PN code buffer, a second input coupled to the input memory, and an output;

a pilot accumulator having an input coupled to the output of the first multiplier, and an output;

a pilot memory coupled to the first accumulator;

a channel estimator coupled to the pilot memory;

a peak detector coupled to the pilot memory;

a data accumulator coupled to the data multiplier;

load controller having a first input coupled to the peak detector, a second input coupled to data accumulator, and an output;

a data memory coupled to the load controller;

a phase rotator having a first input coupled to the channel estimator, a second input coupled to the data memory, and an output; and

a symbol combiner having an input coupled to the phase rotator, and an output which provides the symbol output.

2. The chip rate base band processor of claim 1 further comprising a cluster tracker having an input coupled to the pilot memory, and an output coupled to the pilot PN code buffer.

3. The chip rate base band processor of claim 1 wherein the output of the cluster tracker is coupled to the data PN code buffer.

4. A chip rate base band processor which receives digital information containing symbol information and provides a symbol output, comprising:

an input memory which stores the digital information;

a pilot correlator having an input coupled to the input memory, and an output;

a data correlator having an input coupled to the input memory, and an output;

a pilot memory coupled to the pilot correlator;

a channel estimator having an input coupled to the pilot memory, and an output;

a data memory having an input coupled to the data correlator;

a phase rotator having a first input coupled to the output of the channel estimator, a second input coupled to the data memory, and an output; and

a symbol combiner having an input coupled to the output of the phase rotator, and an output which provides the symbol output.

5. The chip rate base band processor of claim 4 further comprising a second data correlator coupled to the input memory.

6. The chip rate base band processor of claim 5 further comprising:

a second data memory coupled to the second data correlator;

a second phase rotator having a first input coupled to the output of the channel estimator, a second input coupled to the second data memory, and an output; and

a second symbol combiner having an input coupled to the output of the phase rotator, and an output which provides the symbol output.

7. In a chip rate base band processor which receives digital information containing symbol information, wherein each symbol of the symbol information is of a predetermined time duration, a method comprising the steps of:

storing the digital information;

multiplying a PN code with a first segment, representative of the predetermined time duration, of the stored digital information and

multiplying the PN code with a second segment, representative of the predetermined time duration, of the stored digital information.

8. In a chip rate base band processor which receives digital information containing symbol information, wherein each symbol of the symbol information is of a predetermined time duration, a method comprising the steps of:

storing the digital information; and

successively multiplying a first PN code with a first plurality of segments of the stored digital information, wherein each segment is representative of the predetermined time duration.

9. The method of claim 8 further comprising successively multiplying a pilot PN code with the first plurality of segments of the stored digital information.

10. The method of claim 8, wherein the first PN code is a data code.

11. The method of claim 8, wherein the first PN code is a pilot code.

12. The method of claim 8, further comprising multiplying a second PN code with a second plurality of segments of the stored digital information, wherein each segment is representative of the predetermined time duration.

13. The method of claim 12, wherein the first PN code and the second PN code are data PN codes.

14. The method of claim 13 further comprising:

successively multiplying a first pilot PN code with the first plurality of segments of the stored digital information; and

successively multiplying a second pilot PN code with the second plurality of segments of the stored digital information.

~~15. A chip rate base band~~ processor which receives digital information containing symbol information, wherein each symbol of the symbol information is of a predetermined time duration, a method comprising the steps of:

a memory which stores digital information representative of a plurality of the predetermined time durations;

a first multiplier coupled to the memory; and

a first PN code buffer coupled to the first multiplier.

16. The chip rate base band processor further comprising a incrementer means for successively outputting a portion of the digital information from the memory to the multiplier in segments representative of the predetermined time duration.

17. The chip rate base band processor of claim 16 further comprising:

a second multiplier coupled to the memory; and

a second PN code buffer coupled to the second multiplier.